In the Claims

Applicant submits below a complete listing of the current claims, including marked-up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing. This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims

1. (Previously Presented) A method of ordering variables of a binary decision diagram representation of a hardware system, comprising acts of:

arranging the variables of the binary decision diagram in a representation of a graph, corresponding to the hardware system, the graph having a top, nodes and leaves, the nodes being labeled with the variables of the binary decision diagram and the leaves being labeled with a set of functions, thereby to generate labels for the nodes and leaves, whereby the set of functions labeling the leaves reachable from one of the nodes corresponds to the set of functions that depend on the variables labeling the one of the nodes;

traversing the representation of the graph from the top down to produce a list of labels in a selected order; and

using the selected order of the list to determine a sifting order in which the variables are to be sifted to restructure the binary decision diagram representation of the hardware system prior to sifting the variables.

2. (Previously Presented) An apparatus for ordering variables of a binary decision diagram representation of a hardware system, comprising :

a first storage circuit to store first bits representing the variables of the binary decision diagram;

a second storage circuit; and

a processor, coupled to the first storage circuit and the second storage circuit, programmed to arrange the variables of the binary decision diagram in a representation of a graph having a top, nodes, and leaves, and to generate labels for the nodes and leaves, the nodes being labeled with the variables of the binary decision diagram and the leaves being labeled with

a set of functions, the set of functions labeling the leaves reachable from one of the nodes corresponding to the set of functions which depend on the variables labeling the one of the nodes, the processor also being programmed to traverse the representation of the graph from the top down, and to output to the second storage circuit a list of labels in a selected order based upon traversal of the representation of the graph prior to sifting the variables according to the selected order.

3. (Previously Presented) A method of restructuring a binary decision diagram representative of a hardware system, the binary decision diagram including a plurality of variables, the method comprising acts of:

arranging variables of the binary decision diagram in a representation of a graph corresponding to the hardware system, the graph having a top, nodes, and leaves, to generate labels for the nodes and leaves, the nodes being labeled with the variables of the binary decision diagram and the leaves being labeled with a set of functions, the set of functions labeling the leaves reachable from one of the nodes corresponding to the set of functions which depend on the variables labeling the one of the nodes;

traversing the representation of the graph from the top down to produce a list of the labels in a selected order;

sifting the variables based on the selected order; and

restructuring the binary decision diagram based on the act of sifting the variables.

4. (Previously Amended) The method of claim 3, wherein the variables are sifted one-by-one to a deepest location.

5. (Previously Amended) The method of claim 3, wherein the variables are sifted one-by-one in the selected order to a deepest location followed by sifting in reverse order to a shallowest location.

6. (Previously Presented) An apparatus for restructuring a binary decision diagram representative of a hardware system, comprising:

storage circuitry for storing bits representative of a set of functions as a binary decision diagram corresponding to the hardware system, the binary decision diagram having a plurality of nodes, the nodes being labeled with variables to provide labels for the nodes; and

a processor adapted to detect a number of nodes of the binary decision diagram, and in response to the detection,

arranging the variables of the binary decision diagram ~~on~~ in a representation of a graph having a top, nodes and leaves, to generate labels for the nodes and leaves, the nodes being labeled with the variables of the binary decision diagram and the leaves being labeled with a set of functions, the set of functions labeling the leaves reachable from one of the nodes corresponding to the set of functions which depend on the variables labeling the one of the nodes,

traversing the representation of the graph from the top down, to produce a list of the labels in a selected order, and

sifting the variables of the binary decision diagram based on the selected order, wherein the sifted variables are written by the processors to the storage circuitry.

7. (Previously Presented) A method for proving the properties of a hardware system, the hardware system comprising a plurality of internal signals, wherein a plurality of functions determine variables of the internal signals, the method comprising acts of:

representing the hardware system as a binary decision diagram having a plurality of nodes, the nodes being labeled with variables to provide labels for the nodes;

substituting the functions which determine the variables of the internal signals;

arranging the variables of the binary decision diagram ~~on~~ in a representation of a graph having a top, nodes and leaves, the nodes being labeled with the variables of the system and the leaves being labeled with a set of functions to generate labels for the nodes and leaves, whereby the set of functions labeling the leaves reachable from one of the nodes corresponds to the set of functions which depend on the variables labeling the one of the nodes;

traversing the representation of the graph from the top down to produce a list of the labels in a selected order; and

sifting the variables of the binary decision diagram based on the selected order.

8. (Previously Presented) An apparatus for proving properties of a hardware system, the hardware system comprising a plurality of internal signals, wherein a plurality of functions determine values of the internal signals, the apparatus comprising:

first storage circuitry for storing bits representative of a set of functions which represent the hardware system as a binary decision diagram having a plurality of nodes, the nodes being labeled with variables to provide labels for the nodes;

a processor that substitutes the functions which determine the values of the internal signals into the set of functions representing the system and detects an increase in a number of the nodes of the binary decision diagram, and in response to the detection, arranges the variables of the binary decision diagram ~~on~~ in a representation of a graph having a top, nodes and leaves, the nodes being labeled with ~~a~~ the set of functions to generate labels for the nodes and leaves, whereby the set of functions labeling the leaves reachable from one of the nodes corresponds to the set of functions which depend on the variables labeling the one of the nodes, traverses the labels in a selected order and sifts the variables of the binary decision diagram based on the selected order; and

second storage circuitry, wherein the sifted variables of the binary decision diagram are written by the processor to the second storage circuitry.

9. (Previously Amended) The apparatus of claim 8, wherein the number is a threshold derived from an original number of nodes.

10. (Previously Amended) Apparatus as claimed in claim 8, wherein the number is a number of nodes which branch on a predetermined variable.

11. (Previously Amended) The apparatus of claim 8, wherein the number is an absolute number.

12. (New) The method of claim 1, wherein one or more of the acts of arranging, traversing and using are implemented using a computer.

13. (New) The method of claim 12, wherein the acts of arranging, traversing and using are implemented using a computer.

14. (New) The method of claim 3, wherein one or more of the acts of arranging, traversing, sifting and restructuring are implemented using a computer.

15. (New) The method of claim 14, wherein the acts of arranging, traversing, sifting and restructuring are implemented using a computer.

16. (New) The method of claim 7, wherein one or more of the acts of arranging, traversing and sifting are implemented using a computer.

17. (New) The method of claim 16, wherein the acts of arranging, traversing and sifting are implemented using a computer.